IN THE CLAIMS:

Claims 1-22 (Cancel without prejudice or disclaimer)

23. (Original) A process for fabricating an integrated circuit, comprising:

forming a gate structure over a substrate, said gate structure having a length of approximately 1.25 μm or less; and

forming a source and a drain, said source and said drain not having lightly doped regions.

24. (Original) A process for fabricating an integrated circuit as recited in claim 23, wherein said process further comprises forming a channel before forming said source and said drain.

25. (Original) A process as recited in claim 23, wherein said forming said gate structure further comprises:

forming an oxide layer over said substrate; and

forming a conductive layer over said oxide layer.

26. (Original) A process as recited in claim 24, wherein said channel is doped by a halo implantation.

27. (Original) A process as recited in claim 23, wherein said length is in the range of approximately 0.25 μm to approximately 0.05 μm.

28. (Original) A process as recited in claim 25, wherein said oxide layer has a first oxide portion and a second oxide portion.

29. (Original) A process as recited in claim 23, wherein a spacer is not formed adjacent said gate structure.

30. (Original) A process as recited in claim 25, wherein said oxide layer has a thickness in the range of approximately 1.5 nm to approximately 20.0 nm.

31. (Original) A process as recited in claim 23, wherein said source and said drain having doping levels in the range of approximately $1X10^{20}/cm^3$ to $5X10^{20}/cm^3$.

32. (Original) A process as recited in claim 24, wherein said channel has a doping level in the range of approximately $1X10^{16}/cm^3$ to approximately $1X10^{19}/cm^3$.

33. (Original) A process for fabricating an integrated circuit, comprising:

forming an oxide layer over a substrate;

forming a conductive layer over said oxide layer, said oxide layer and said conductive layer forming a gate having a length of 1.25 μm or less;

forming a channel in said substrate; and

forming a source and a drain, said source and said drain not having lightly doped regions.

34. (Original) A process as recited in claim 33, wherein said channel is doped by a halo implantation.

35. (Original) A process as recited in claim 33, wherein said length is in the range of approximately 0.25 μm to approximately 0.05 μm.

36. (Original) A process as recited in claim 33, wherein said oxide layer has a first oxide portion and a second oxide portion.

37. (Original) A process as recited in claim 33, wherein a spacer is not formed adjacent said gate structure.

38. (Original) A process as recited in claim 33, wherein said oxide layer has a thickness in the range of approximately 1.5 nm to approximately 20.0 nm.

39. (Original) A process as recited in claim 33, wherein said source and said drain having doping levels in the range of approximately $1X10^{20}/cm^3$ to approximately $5X10^{20}/cm^3$.

40. (Original) A process as recited in claim 33, wherein said channel has a doping level in the range of approximately $1X10^{16}/cm^3$ to approximately $1X10^{19}/cm^3$.